AMENDMENTS TO THE CLAIMS

Upon entry of the present amendment, the status of the claims will be as is shown below. This listing of claims replaces all previous versions and listings of claims in the present application.

Listing of Claims:

1-12. (Cancelled)

13. (Previously Presented) An information processing device, comprising:

a DRAM having a burst mode which burst-transfers data of successive column addresses;

at least one data processor operable to issue an access request; and

an address converter operable to convert access addresses which are included in the access request issued from said at least one data processor,

wherein at least one of said at least one data processor is operable to access an M × N rectangular area, where M and N are positive integers,

said address converter is operable to convert access addresses so that a column address of data at a (K+m)th column of an Lth line and a column address of data at a Kth column of an (L+n)th line become successive, where K, m, L, and n are positive integers, $m \leq M$, and $n \leq N$, and

at least one rectangular area of said DRAM is a frame memory which stores image data, the at least one rectangular area is M pixels × N lines in the image data, and

said at least one data processor is operable to perform one of motion compensation and motion estimation, where n=2n' and n' is a positive integer,

wherein the DRAM burst-transfers the data at the (K+m)th column of the Lth line and the data at the Kth column of the (L+n)th line in the burst mode by successively accessing the column address of the data at the (K+m)th column of the Lth line and the column address of the data at the Kth column of the (L+n)th line.

14. (Previously Presented) The information processing device according to Claim 13,

wherein another data processor is operable to access the image data on a line basis, and to continuously read out data of all 2n lines.

15. (Currently Amended) The information processing device according to Claim 13,

wherein said at least one data processor is operable to decode an inputted stream on a basis of at least two macroblocks, by motion compensation,

said DRAM is operable to store the image data decoded by said at least one data processor,

said information processing device further comprises:

a memory featuring a smaller storage capacity and a faster access speed than said DRAM;

a data transferor operable to transfer the data from said DRAM to said memory, and

said at least one data processor is operable to access the image data stored

in said DRAM as reference data.

16. (Currently Amended) The information processing device according to Claim 15,

wherein the image data stored in said DRAM is split into transfer regions larger in size than the at least one rectangular area, and

said data transferor is operable to transfer data on a transfer region basis from said DRAM to said memory, based on the access request from said at least one data processor.

17. (Currently Amended) The information processing device according to Claim 15,

wherein said data transferor is operable to transfer a minimum area which surrounds plural rectangular areas as a transfer region as data from said DRAM to said memory, based on [[an]] the access request from said at least one data processor.

18. (Previously Presented) The information processing device according to Claim 16,

wherein said data transferor includes a register which holds a size of the transfer region.

19. (Previously Presented) The information processing device according to Claim 16,

wherein said data transferor is operable to transfer the data from said DRAM to said memory when a predetermined number n1 of access requests are outputted from said

at least one data processor.

20. (Previously Presented) The information processing device according to Claim 19,

wherein said data transferor includes a register which holds the size of the transfer region and the predetermined number n1.

21. (Previously Presented) The information processing device according to Claim 16,

wherein said data transferor is operable to transfer the transfer region which includes all rectangular areas, from said DRAM to said memory when access requests from said at least one data processor request the rectangular areas which are adjacent or overlapping.

22. (Currently Amended) The information processing device according to Claim 16, wherein said at least one data processor includes:

a motion vector estimator operable to estimate plural motion vectors corresponding to plural macroblocks from an inputted stream; and

a decoder operable to decode the inputted stream on a macroblock basis, and to store a decoding result into said DRAM,

wherein a decoding sequence of the plural macroblocks is changed based on the plural motion vectors so that addresses for accessing said DRAM become successive.

23. (Currently Amended) A data access method for accessing a rectangular

area made up of M pixels × N lines in image data from a DRAM, the DRAM having a burst mode which burst-transfers data of continuous column addresses, and storing the image data, the data access method comprising:

inputting an access request for the rectangular area; ~~and~~

converting access addresses included in the access request so that a column address of data at a (K+m)th column of an Lth line and a column address of data at a Kth column of an (L+n)th line become successive, where K, m, L, and n are positive integers, $m \leq M$, and $n \leq N$; and

burst-transferring the data at the (K+m)th column of the Lth line and the data at the Kth column of the (L+n)th line in the burst mode by successively accessing the column address of the data at the (K+m)th column of the Lth line and the column address of the data at the Kth column of the (L+n)th line,

wherein at least one area of said DRAM is a frame memory which stores image data and the rectangular area is M pixels × N lines in the image data, where M and N are positive integers, and a data processor performs motion compensation and motion estimation, where n=2n' and n' is a positive integer.

24. (Previously Presented) The information processing device according to Claim 17,

wherein said data transferor is operable to transfer the data from said DRAM to said memory when a predetermined number n1 of access requests are outputted from said data processor.

25. (Previously Presented) The information processing device according to Claim 24,

wherein said data transferor includes a register which holds a size of the transfer region and the predetermined number n1.

26. (Previously Presented) The information processing device according to Claim 17,

wherein said data transferor is operable to transfer the transfer region which includes all rectangular areas, from said DRAM to said memory when access requests from said at least one data processor request the rectangular areas which are adjacent or overlapping.